­**Requirements for Microcontroller IF (Prefix: MCI)**

**Reset Condition:**

MCI\_RES\_01. ‘o\_reg\_data[31:0]” shall output all 0s when ‘i\_reset’ is 1.

MCI\_RES\_02. ‘o\_reg\_w\_bus[31:0]’ shall output all 0s when ‘i\_reset’ is 1.

MCI\_RES\_03. ‘o\_rs\_vector[30:0]’ shall output all 0s when ‘i\_reset’ is 1.

MCI\_RES\_04. ‘o\_r\_neg\_w’ shall output 0 when ‘i\_reset’ is 1.

MCI\_RES\_05. ‘o\_ack’ shall output 0 when ‘i\_reset’ is 1.

MCI\_RES\_04. ‘o\_error’ shall output 0 when ‘i\_reset’ is 1.

**Read Operation:**

1. ‘o\_reg\_data’ shall read the data from ‘i\_reg\_r\_data’ when ‘i\_cs’ ,‘i\_r\_neg\_w’ are both set to ‘1’ and the read address ‘i\_addr’ is valid, else it outputs all 0s. (Valid address in read operation : 0x000，0x004，0x008，0x00c，0x010，0x014，0x018，0x01c，0x020, 0x050, 0x054, 0x058, 0x05c, 0x060, 0x064, 0x068, 0x06c, 0x070, 0x074, 0x078, 0x07c, 0x080)
2. Module shall read signal from ‘i\_reg\_ack’ and output through ‘o\_ack’
3. Module shall read signal from ‘i\_r\_neg\_w’ and output through ‘o\_r\_neg\_w’.
4. ‘o\_rs\_vector[0]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x000’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
5. ‘o\_rs\_vector[1]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x004’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
6. ‘o\_rs\_vector[2]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x008’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
7. ‘o\_rs\_vector[3]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x00C’ ,ootherwise ‘o\_rs\_vector’ is set to all 0s
8. ‘o\_rs\_vector[4]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x010’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
9. ‘o\_rs\_vector[5]’ shall only be set to 1 for one clock cycle‘ i\_cs’ if ‘i\_cs’ and ‘i\_neg\_w’ are 1 and‘i\_addr’ is ‘0x014’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
10. ‘o\_rs\_vector[6]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x018’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
11. ‘o\_rs\_vector[7]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x01C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
12. ‘o\_rs\_vector[8]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x020’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
13. ‘o\_rs\_vector[18]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x050’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
14. ‘o\_rs\_vector[19]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x054’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
15. ‘o\_rs\_vector[20]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x058’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
16. ‘o\_rs\_vector[21]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x05C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
17. ‘o\_rs\_vector[22]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x060’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
18. ‘o\_rs\_vector[23]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x064’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
19. ‘o\_rs\_vector[24]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x068’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
20. ‘o\_rs\_vector[25]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x06C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
21. ‘o\_rs\_vector[26]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x070’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
22. ‘o\_rs\_vector[27]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x074’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
23. ‘o\_rs\_vector[28]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x078’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
24. ‘o\_rs\_vector[29]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x07C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
25. ‘o\_rs\_vector[30]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ and ‘i\_neg\_w’ are 1 and ‘i\_addr’ is ‘0x080’ ,otherwise ‘o\_rs\_vector’ is set to all 0s

**Write Operation:**

1. ‘o\_reg\_w\_bus’ shall output data from ‘i\_bus\_data’ when i\_cs is 1, i\_r\_neg\_w is 0, and the write address is valid, else it retains its previous value. (Valid address in write operation : 0x000，0x004，0x008，0x00c，0x014, 0x020,0x024, 0x030, 0x034, 0x038, 0x03c, 0x040, 0x044, 0x048, 0x04c, 0x060, 0x064, 0x068, 0x06c, 0x070, 0x074, 0x078, 0x07c, 0x080)
2. Module shall read signal from ‘i\_reg\_ack’ and output through ‘o\_ack’
3. Module shall read signal from ‘i\_r\_neg\_w’ and output through ‘o\_r\_neg\_w’.
4. ‘o\_rs\_vector[0]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x000’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
5. ‘o\_rs\_vector[1]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x004’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
6. ‘o\_rs\_vector[2]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x008’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
7. ‘o\_rs\_vector[3]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x00C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
8. ‘o\_rs\_vector[5]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x014’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
9. ‘o\_rs\_vector[8]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x020’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
10. ‘o\_rs\_vector[9]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x024’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
11. ‘o\_rs\_vector[10]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x030’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
12. ‘o\_rs\_vector[11]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x034’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
13. ‘o\_rs\_vector[12]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x038’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
14. ‘o\_rs\_vector[13]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x03c’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
15. ‘o\_rs\_vector[14]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x040’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
16. ‘o\_rs\_vector[15]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x044’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
17. ‘o\_rs\_vector[16]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x048’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
18. ‘o\_rs\_vector[17]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x04c’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
19. ‘o\_rs\_vector[22]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x060’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
20. ‘o\_rs\_vector[23]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x064’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
21. ‘o\_rs\_vector[24]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x068’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
22. ‘o\_rs\_vector[25]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x06C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
23. ‘o\_rs\_vector[26]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x070’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
24. ‘o\_rs\_vector[27]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x074’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
25. ‘o\_rs\_vector[28]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x078’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
26. ‘o\_rs\_vector[29]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x07C’ ,otherwise ‘o\_rs\_vector’ is set to all 0s
27. ‘o\_rs\_vector[30]’ shall only be set to 1 for one clock cycle if i\_sys\_clk transitions from 0 to 1 while ‘i\_cs’ is 1, ‘i\_neg\_w’ is 0 and ‘i\_addr’ is ‘0x080’ ,otherwise ‘o\_rs\_vector’ is set to all 0s

**Error condition**

MCI\_ER\_01.Module shall read signal from i\_reg\_error and output through ‘o\_error’